BASIS OF ELECTROMAGNETIC COMPATIBILITY OF INTEGRATED CIRCUIT

Chapter IV - OVERVIEW OF EMC ISSUES

Corrections of exercises

I. EXERCISE NO 1 - CROSSTALK

Two close microstrip lines are drawn on a 0.4 mm thick FR4 printed circuit board (εr = 4.5). The lines are 0.5 mm wide, 5 cm long, and separated by a 0.25 mm gap. They are made of 35 µm thick copper traces. One line is excited by a driver, while the second is quiet and is the victim line. This exercise aims at computing the maximum amplitude of the noise coupled on the victim line due to crosstalk.

1. Compute the per-unit-length parameters of the coupled microstrip lines. You can use the IC-EMC Interconnect Parameters tool.Give the single-ended characteristic impedance of each microstrip line and the propagation delay.The lines are assumed lossless.

2. The driver produces a square signal with the following characteristics:

- Min voltage Vmin = 0 V, Max voltage Vmax = 2.5 V
- Period = 20 ns, duty cycle = 50 %
- Rise and fall time Tr and Tf = 2 ns

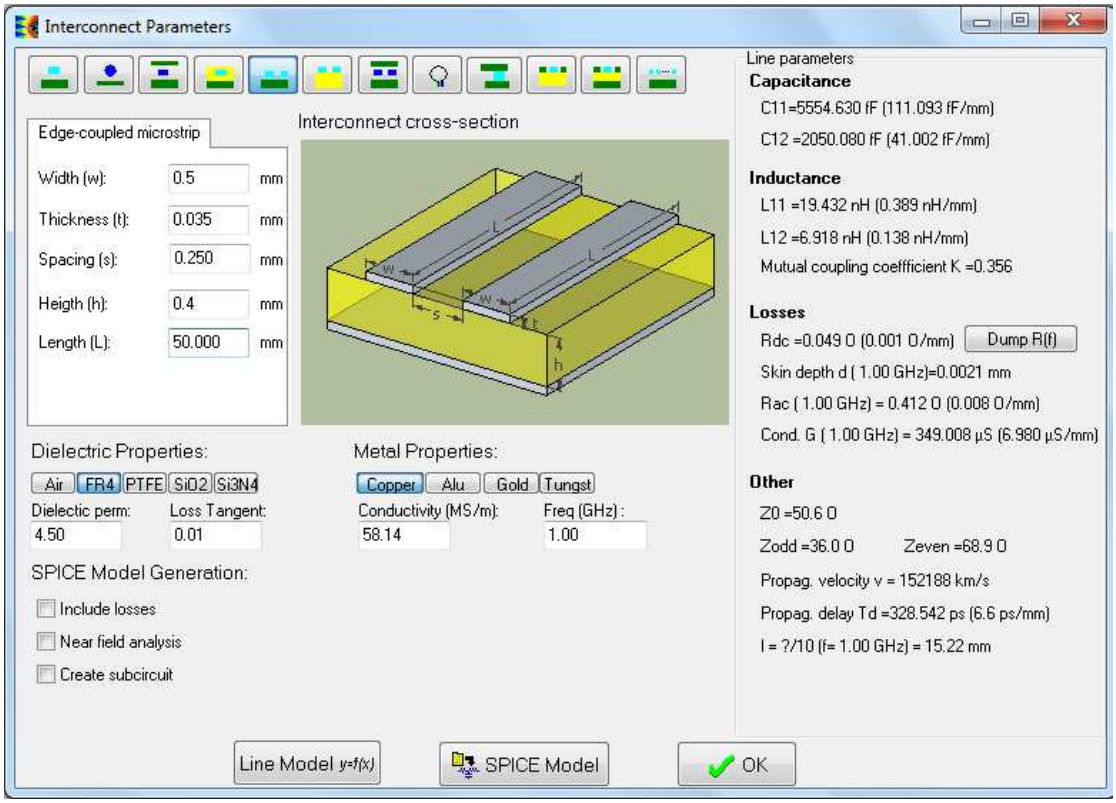
Every line termination is loaded by 50 ohms. Is matching critical for these lines?

3. Estimate the near-end and far-end voltage amplitudes on the quiet line terminations. Are near-end and far-end voltages symetrical?

4. With the IC-EMC - Interconnect Parameter tool, build an electrical model of the line which is valid up to 1 GHz (button SPICE model). Add the model of the driver and the termination resistance. Simulate and compute the near-end and far-end voltage transient waveforms on the quiet line terminations.Compare with results of question 3.

Corrections:

1. Use Tools / Interconnects Parameters:



Self capacitance c11 = 111 fF/mm, mutual capacitance c12 = 41 fF/mm

Self inductance l11 = 0.39 nH/mm, mutual inductance l12 = 0.14 nH/mm

The single-ended mode characteristic impedance Z0 = 51 Ω and the propagation delay Td = 329 ps.

2. According to the rule of thumb given by equation 4-5, signal integrity (SI) issues become critical if line with a propagation delay Td are excited by signals with a transition time Tr such as Td < Tr/10. As the propagation delay Td is 321 ps and the rise and fall times Tr and Tf are equal to 2 ns, SI issues become critical, so the line impedance and termination matching must be controlled.

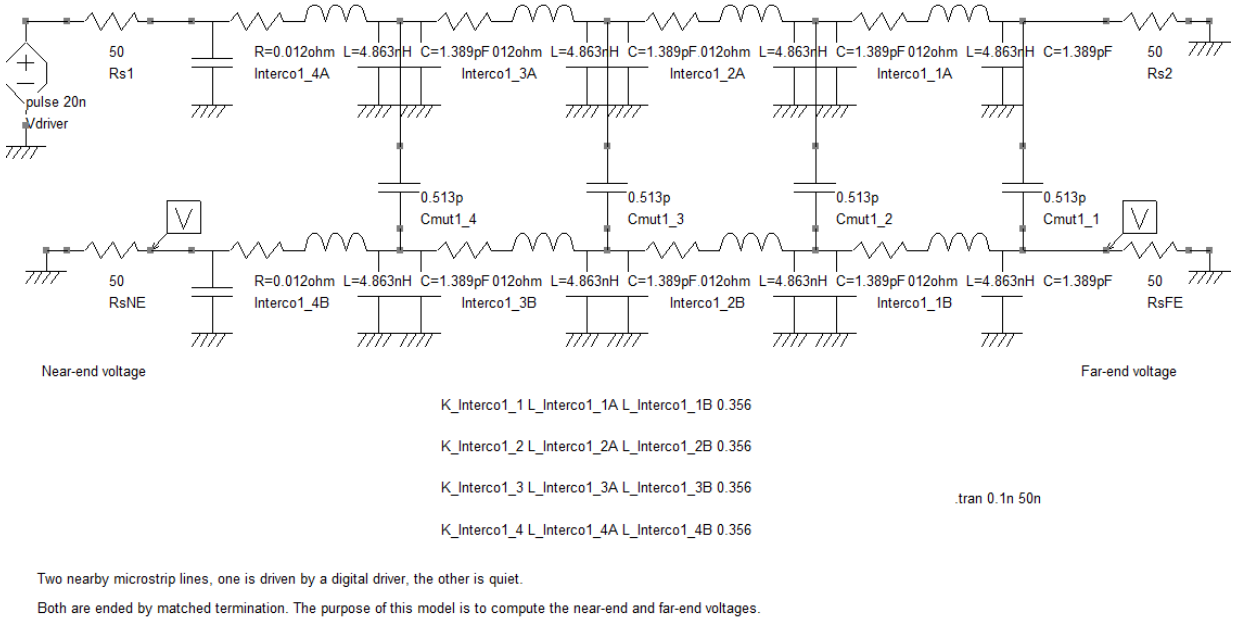
3. As the microstrip line terminations are matched and if we assume that the coupling between the lines is weak, the near-end and far-end voltages can be estimated according to equations 4-11 and 4-12:

Near-end voltage amplitude: $V_{NE\max} = \pm\frac{T_d}{2}\left(\frac{C_{12}}{C_{11}+C_{12}} + \frac{L_{12}}{L_1}\right)\frac{V_{\max}-V_{\min}}{2T_r} = \pm 64mV$

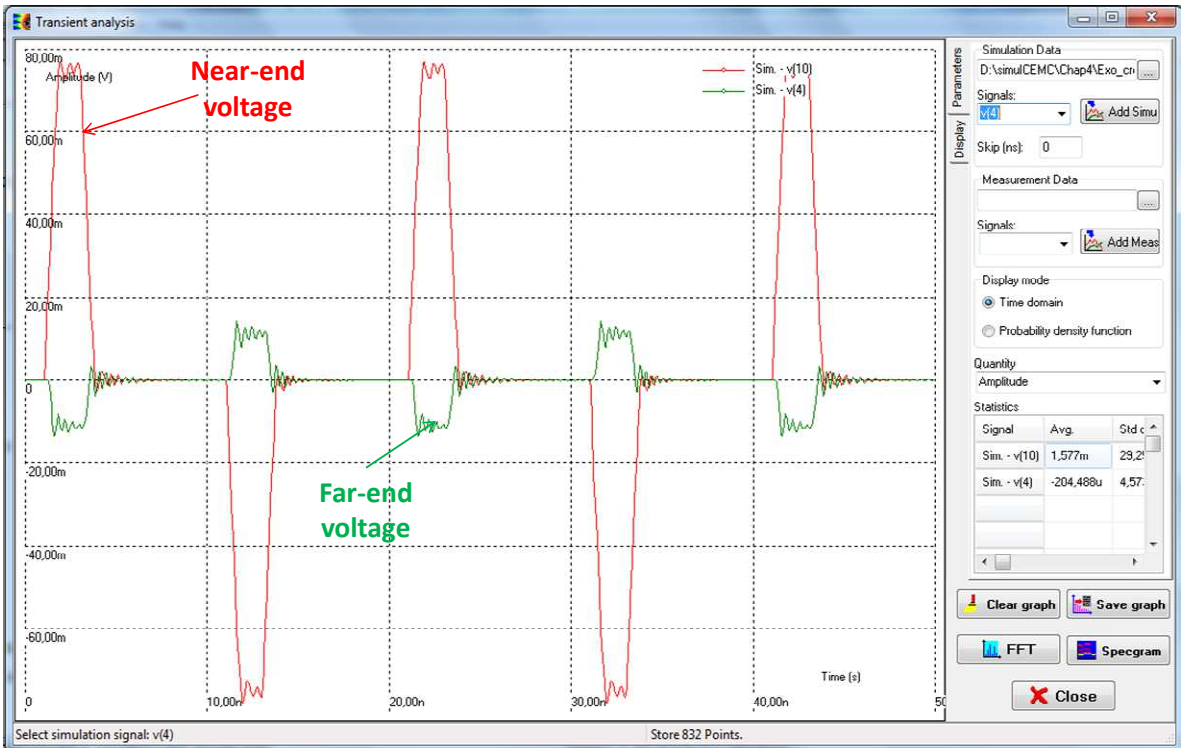
Far-end voltage amplitude: $V_{FE\max} = \pm\frac{T_d}{2}\left(\frac{C_{12}}{C_{11}+C_{12}} - \frac{L_{12}}{L_1}\right)\frac{V_{\max}-V_{\min}}{T_r} = \mp 9mV$

Both voltages have opposite signs and different amplitude since the electrical and magnetic coupling contributions are not combined identically at each end. At near-end, electrical and magnetic coupling contributions add up. Oppositely, they substract at far-end. If the ratios $\frac{C_{12}}{C_{11}+C_{12}}$ and $\frac{L_{12}}{L_1}$ were equal, they could cancel and far-end voltage would disappear.

4. From Tools / Interconnect Parameters, be sure that there is '1.00' in the field 'Freq (GHz)' and click on the button SPICE Model to generate automatically the RLC equivalent circuit of the coupled microstrip. Then, place termination resistors and the excitation voltage. Set a transient simulation with a sufficient duration to observe several periods of the driver signal. The electrical schematic diagram model is given in the file Coupled_microstrip.sch and is shown below.



Launch the SPICE simulation by clicking on , either with LTSPICE or WinSPICE. At the end of the simulation, click on EMC / Voltage vs. Time or on . The simulated near-end and far-end voltages are presented below.



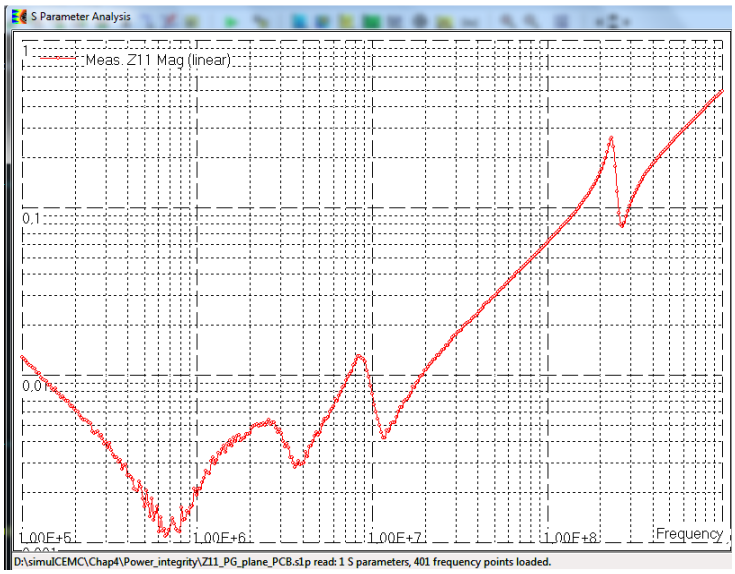
Short impulses arise during transitions of the driver signal. The amplitude of the near-end voltage is +/- 73 mV. The amplitude of the far-end voltage is +/- 11 mV. Near-end and far-en voltage have opposite signs and alternate at each excitation signal transition. The simulated amplitudes correlate with the estimated ones. Differences can be explained by the non-perfect matching of the lines and by the weak coupling assumption.

II. EXERCISE NO 2 - POWER INTEGRITY OF A DIGITAL CIRCUIT

The first version of the design of an electronic board for a digital application is over and you have to validate this design before making the PCB. A major concern is the power integrity issue. Among all the devices mounted on this PCB, an FPGA works as the main contributor of dynamic current consumption of the application. This microprocessor is designed in low power CMOS28 nm technology. It is supplied by a 1.2 V regulated voltage.

The FPGA is mounted in a 324 pin BGA package. The operating frequency is set to 80 MHz by an on-chip clock. Numerous I/O buffers and high speed interfaces will be activated in the final application.

The following figure provides a simulation of the impedance profile in the frequency domain measured between a power and ground plane of the PCB. In the model, all the decoupling capacitors are assembled, except the FPGA. The measurement file is given by the Z11_PG_plane_PCB.s1p file.

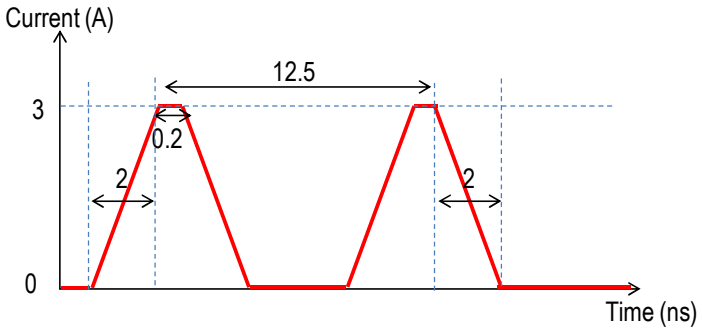


1. From the impedance measurement, build an equivalent electrical model of the power-ground plane which is valid up to 1 GHz.

2. The average current consumption of the FPGA is estimated to 1 A. Suggest a target impedance for the power-ground plane impedance.

3. Considering the target impedance chosen in the previous question, do you think that the board is sufficient? Is the target impedance a conservative criterion? Is there any problematic frequency range for power integrity?

3. The figure below gives an estimation of the dynamic current consumption of the circuit. What should be the maximum resistance and inductance of the package power and ground pins? What is the most restrictive constraint?

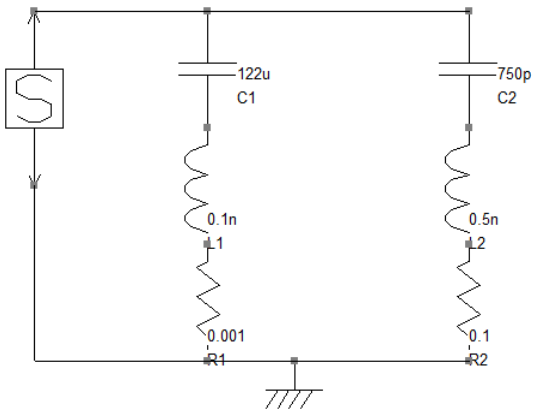


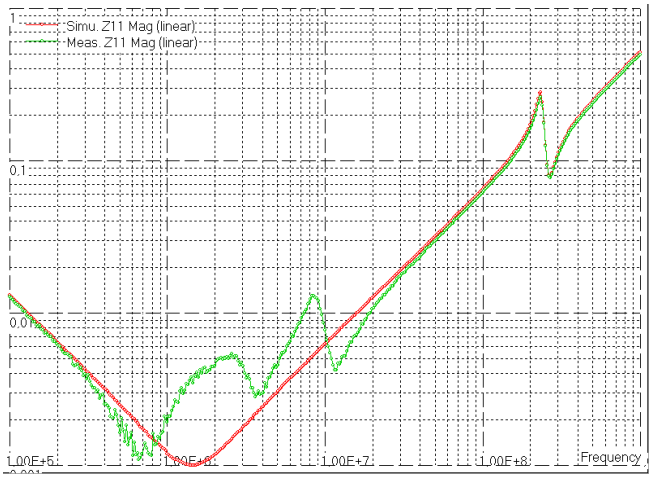
4. Complete the PCB model with the estimation of the current consumption which is needed to simulate the power supply voltage fluctuation. Simulate it in the time and frequency domains. Comment the simulation results.

5. Is the amplitude of the on-chip voltage fluctuation acceptable ? If not, suggest solutions to reduce it.

Corrections:

1. A simple model is given in the file PG_board_model.sch: the decoupling capacitor effect is clearly visible between 100 kHz and several tens of MHz. Numerous resonances are visible due to the large number of capacitors mounted on the board. In this model, only one equivalent RLC branch is added to simulate the effect of decoupling capacitor. The capacitance is extracted from the impedance measured at 100 kHz. The inductance is extracted from the impedance measured at 100 MHz. A second RLC branch is added to model the effect of the power-ground plane. The power-ground plane and the dedcoupling capacitor produces an anti-resonance at 233 MHz. The L and C values of the second branch are adjusted to fit the anti-resonance frequency and the impedance measured at 1 GHz (equation 4-14 can also be used). Its resistance is set adjust the quality factor of this resonator.





Several RLC branches should be added in parallel to improve the modeling of decoupling capacitors and improve the fit between measurement and simulation between 1 MHz and 10 MHz. However, this simple model predicts correctly a very low impedance in this frequency range, where power integrity issues are not critical.

2. The target impedance is the impedance limit for power distribution network to ensure a sufficient power integrity. Equation 4-13 offers a simple method to compute a constant target impedance, equal to the ratio between the maximum allowed power supply voltage fluctuation and the average current consumption. As the circuit power supply is 1.2 V, we can assume that the power supply voltage fluctuation must be limited to 0.12 V (10 % of the nominal supply voltage).The target impedance is equal to: $Z_T = \frac{\Delta V_{dd\,\max}}{I_{av}} = \frac{0.12}{1} = 120 m\Omega$

The target impedance objective is met up to 170 MHz. The circuit activity is synchronized on the 80 MHz on-chip clock. So the current activity will produce a large band frequency content with numerous harmonics of the fundamental frequency at 80 MHz. The amplitude of the harmonics reduces with the order.

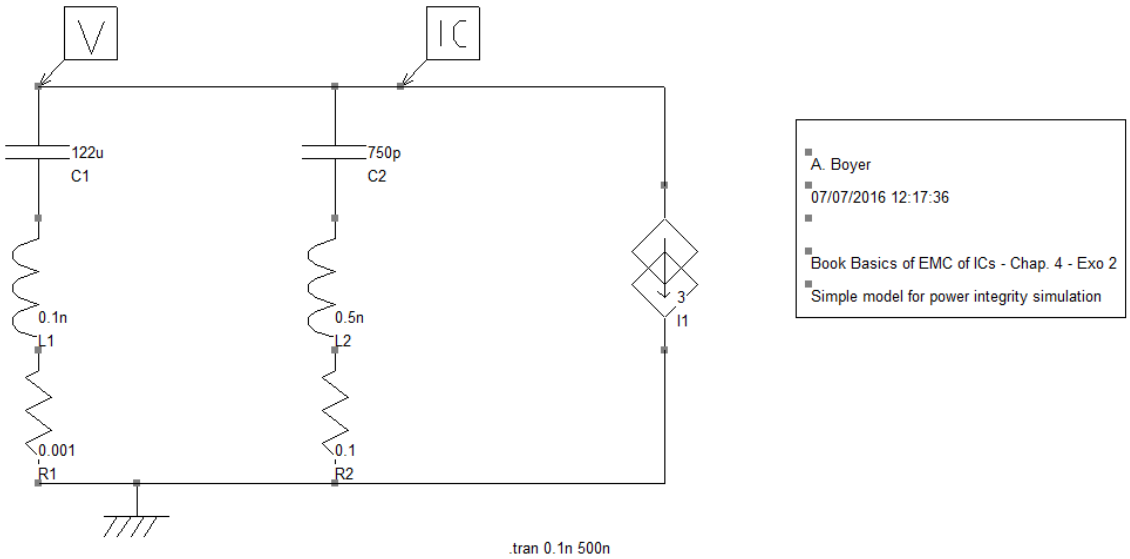
The power-ground plane impedance is small enough on the two first harmonics of the circuit activity, but not for the higher order harmonics. The power-ground plane impedance should be reduced, by increasing the number of decoupling capacitors.

In spite of its simplicity, it should be underlined that the target impedance computed in question 2 gives a very conservative criterion since it considers an average current, and not the spectrum of the actual current produced by the circuit activity.

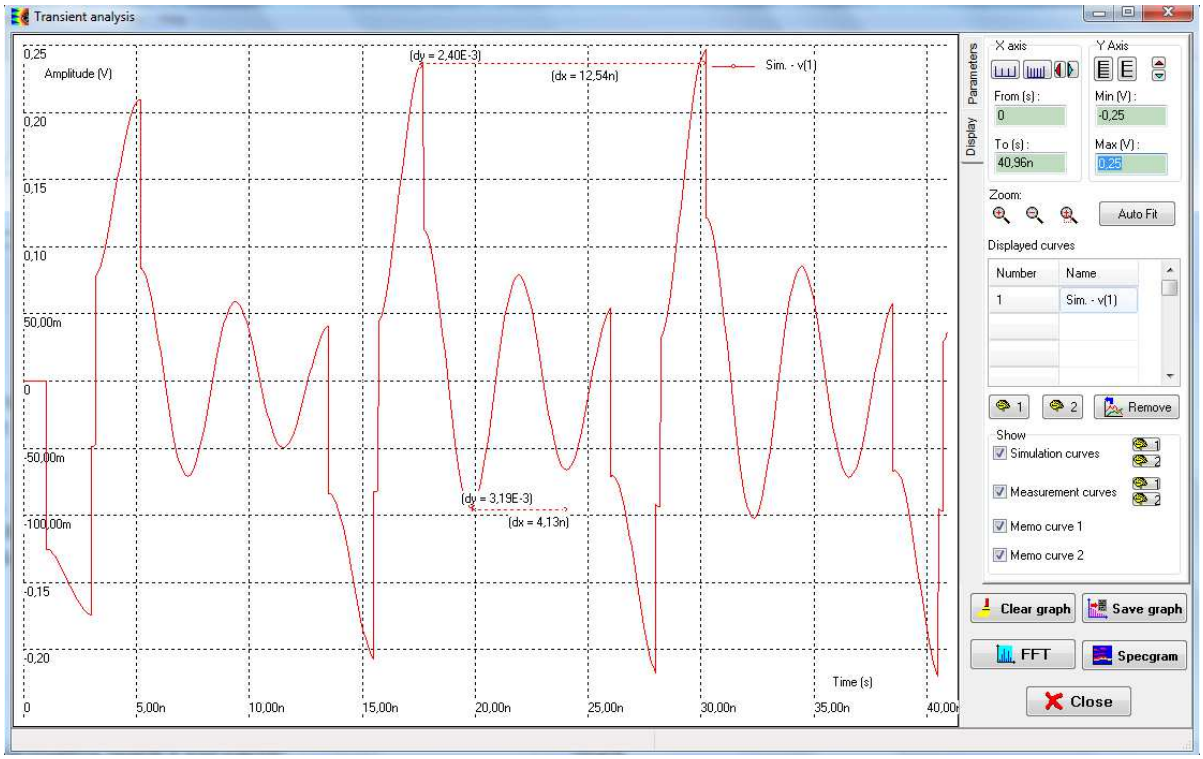
However, a particularly problematic frequency range is visible on the impedance profile: an anti-resonance appears at 230 MHz, due to the PCB and decoupling capacitor, where the power-ground plane impedance becomes large. This anti-resonance frequency is very close to the third hamonic of the on-chip clock, so the circuit activity will certainly excite this frequency. Power integrity will be certainly degraded.

3. Package pins introduce serial resistance and inductance that generate IR drop and delta-I noise (see equation 4-11). To keep a power supply fluctuation less than 120 mV, the maximum serial resistance on power supply and ground pins is: $R < \frac{\Delta V_{DD}}{I_{\max}} = \frac{0.12}{3} = 40 m\Omega$. The maximum serial inductance on power supply and ground pins is: $l < \frac{\Delta V_{DD}}{dI} dt = \frac{0.12 \times 2.10^{-9}}{3} = 80\,pH$ .In practice, delta-I noise dominates. Here, the most restrictive constraint is on the inductance. If we consider a rule of thumb of 3 nH per BGA pin (see chapter X), 38 power supply and ground pins are required to meet this constraint.

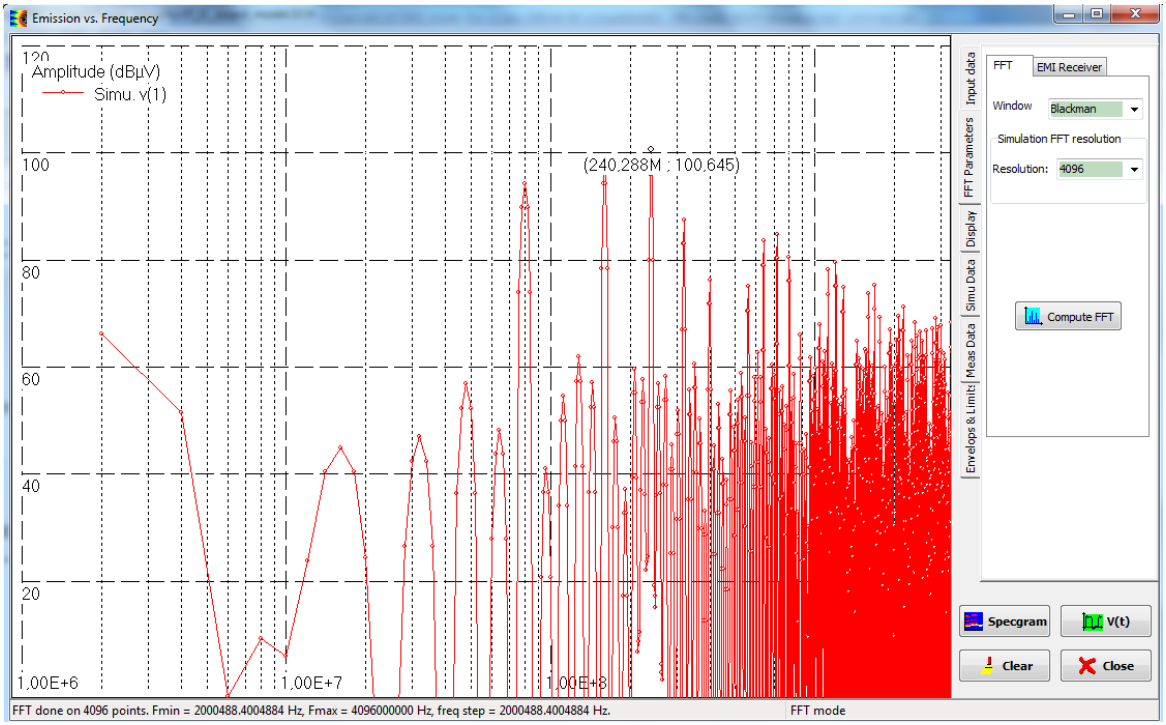
4. Below, the proposed model to simulate the power integrity (PI_IC_board_model.sch). The IC component sets an initial condition on capacitance C1 and C2. Launch the SPICE simulation by clicking on  , either with LTSPICE or WinSPICE.



Result in time domain: click on EMC / Voltage vs. Time or on  . An oscillation with a pseudo-period of about 4.3 ns (i.e. a frequency of 233 MHz) is visible, due to the anti-resonance.



Result in frequency domain: click on EMC / Emission vs. Frequency or on  . the third harmonic (240 MHz) is the highest because it excites the anti-resonance at 233 MHz.



5. The peak-to-peak amplitude of the voltage fluctuation reaches 440 mV, so it is not acceptable (37 % of the nominal power supply). This result is certainly overstimated because the on-chip equivalent capacitance is not taken into account in this model (see chapter XI). This capacitance acts as a local decoupling capacitor.

Several solutions at PCB and IC levels can be proposed to mitigate this problem:

1. at PCB level, increase the number of decoupling capacitors and improve their placement (as close as possible to the FPGA). It will reduce the power-to-ground plane impedance and shift the anti-resonance frequency at a larger frequency.

2. if possible, reduce the dynamic current consumption of the FPGA, i.e. make the FPGA less noisy (action on the source)

3. at IC level, increase the on-chip capacitance, which acts as local decoupling capacitance. As solution 1, it contributes to reduce the PDN impedance.

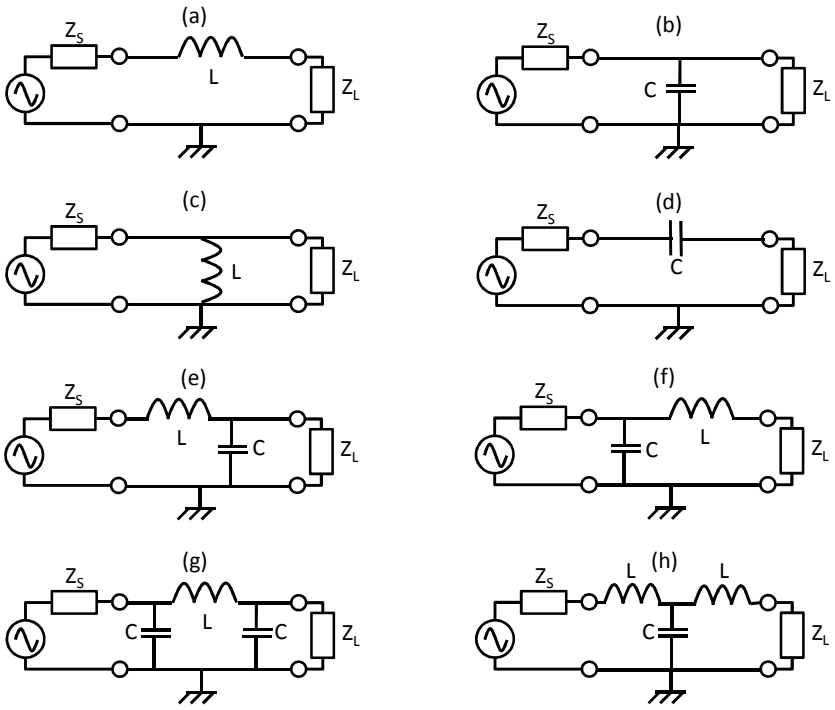
III. EXERCISE NO 3 - POWER INTEGRITY OF A DIGITAL CIRCUIT

EMC filters always stand for low-pass filtering. Their purpose is to attenuate the high-frequency components of an electromagnetic disturbance conducted along a signal or power line, and avoid unwanted radiation. The following figure puts forward eight different basic EMC filter topologies. Filters are placed between a disturbance source and a load Z_L, defined by terminal impedances Z_S and Z_L. In the exercise, it is assumed that the terminal impedances are purely resistive. Three resistance values are considered:

- low impedance - 10 Ω
- medium impedance - 50 Ω
- high impedance - 150 Ω

This exercise aims at comparing different types of EMC filters and determining the conditions on terminal impedances.

A typical indicator of filter effectiveness is the Insertion Loss (IL). It is the ratio of the load voltage without the filter, divided by the load voltage when the filter is connected between the disturbance source and the load. In this exercise, L = 1 µH and C = 10 nF.



1. In the 8 filter configurations presented above, which are EMC filters?

2. Propose a simulation test-bench with IC-EMC to simulate the insertion loss of a filter.

3. For each filter configuration, determine the conditions of terminal impedances which optimize the filter attenuation?

4. Compare the filters in term of roll-off attenuation.

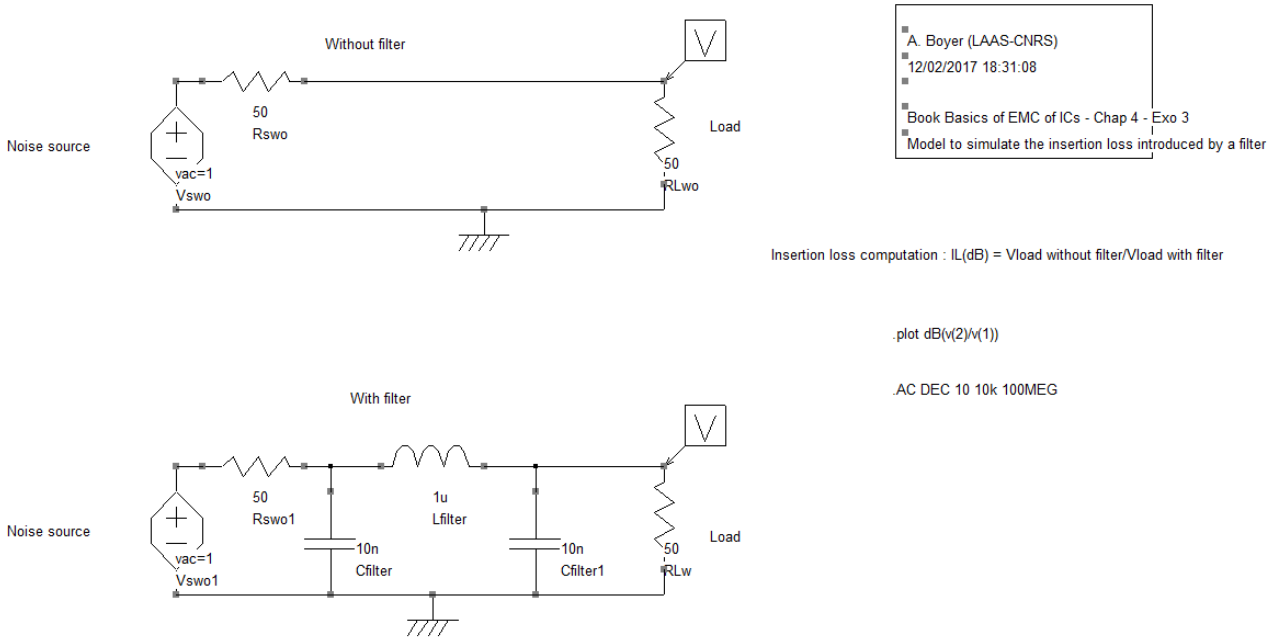
5. Are the predicted filter attenuations realistic? What should be taken into account to predict actual filter attenuation?

Corrections:

1. Except configurations (c) and (d), they are all low-pass filters.

2. Open file Insertion_Loss_Simulation.sch, shown below. The noise source and the load are duplicated. In the top circuit, they are connected directly without filter. In the bottom circuit, the filter is inserted. The insertion loss is computed as the ratio between the load voltages in both circuits,

with the command plot dB(V(2)/V(1)). The result is converted in dB. A small-signal simulation (.AC) is performed to analyze the evolution of the insertion loss in frequency domain.



To study the influence of terminal impedances on insertion loss, change the terminal impedances, simulate the insertion loss and analyze its evolution in frequency domain according to the terminal impedances.

3. Theoretical analyses for the different filter topologies and derivation of the expression of the insertion loss (IL):

(a): Serial inductor: $IL = 1 + j\frac{Z_S Z_L}{Z_S + Z_L} C\omega$. IL is improved for large Z_S and Z_L. This result is confirmed by simulation (better IL value for $Z_S = Z_L = 150\ \Omega$).

(b) :Parallel capacitor: $IL = 1 + j\frac{L\omega}{Z_S + Z_L}$. IL is improved for low Z_S and Z_L. This result is confirmed by simulation (better IL value for $Z_S = Z_L = 10\ \Omega$).

(e): L-type filter: $IL = 1 + \frac{j\omega(L + Z_L Z_S C)}{Z_S + Z_L} - \frac{Z_L LC\omega^2}{Z_S + Z_L} \to -\frac{Z_L LC\omega^2}{Z_S + Z_L}\ if\ \omega \to \infty$. IL is improved for $Z_S >> Z_L$ (only at high frequency). This result is confirmed by simulation (better IL value at high frequency for $Z_L = 10\ \Omega$ and $Z_S = 150\ \Omega$).

(f): L-type filter: $IL \to -\frac{Z_S LC\omega^2}{Z_S + Z_L}\ if\ \omega \to \infty$. IL is improved for $Z_L >> Z_S$ (only at high frequency). This result is confirmed by simulation (better IL value at high frequency for $Z_S = 10\ \Omega$ and $Z_L = 150\ \Omega$).

(g): pi-type filter: $IL = \to -j\frac{Z_L Z_S LC^2\omega^3}{Z_S + Z_L}\ if\ \omega \to \infty$. IL is improved for medium to high Z_S and Z_L (only at high frequency). This result is confirmed by simulation (better IL value at high frequency for $Z_L = 150\ \Omega$ and $Z_S = 150\ \Omega$).

(h): T-type filter: $IL =\rightarrow -j\frac{L^2C\omega^3}{Z_S+Z_L}\ if\ \omega\rightarrow\infty$. IL is improved for low Z_S and Z_L (only at high frequency). This result is confirmed by simulation (better IL value at high frequency for Z_L = 10 Ω and Z_S = 10 Ω).

The theoretical expressions of the insertion losses can be verified with model determined in the first question. Just change the topology of the filter inserted in the bottom circuit.

4. a) and (b): 1st order filter → 20 dB/dec roll-off

(e) and (f): 2nd order filter → 40 dB/dec roll-off

(g) and (h): 3rd order filter → 60 dB/dec roll-off

5. Simulations have been done with ideal inductor and capacitor models. The stray elements of these devices have not been taken into account. However, they change the characteristics of passive devices in frequency domain and thus the attenuation of the filter.

IV. EXERCISE NO 4 - Radiated emission from a SMPS

The conducted emission from the SMPS shown in Fig. 4-15 and its result in Fig. 4-17 are considered in this exercise. The aim is to estimate the radiated emission produced by the circulation of current along the power supply cable between the SMPS and the LISN. The cable length is 1.5 m. The cable is made of two wires 2 mm away from each other.

1. Is the electrically short line approximation verified at 30 MHz?

2. Evaluate the maximum differential-mode radiated emission 3 m away from the SMPS cable at 180 kHz, 8 MHz and 30 MHz.

3. Same question with the common-mode radiated emission.

4. Compare the influence of differential-mode and common-mode currents on the radiated emission. If the 3 m radiated emission limit shown in Fig. 4-22 is considered (EN55022 class A), is the radiated emission of the SMPS with the attached power supply cable acceptable?

Corrections:

1. At 30 MHz, the wavelength is 10 m in air. The length of the cable is 1.5 m, i.e. 1/8th of the wavelength. We can consider that the line is still electrically short at this frequency, but the validity frequency range for this approximation is nearly reached.

2. The maximum electric field produced by the differential-mode current circulating along 2 wires is computed According to equation 4-24:

$$\left|E_D\right|_{\max} = 1.316.10^{-14} \frac{L.d.f^2}{r} I_{DM}$$

Here, we suppose that the power supply cable is electrically short and we neglect the influence of the ground plane. Differential-mode radiated emission at 3 meters:

- At 180 kHz, I_{DM} = 45 dBµA, E_D = 76 pV/m = -82 dBµV/m
- At 8 MHz, I_{DM} = 13 dBµA, E_D = 4 nV/m = -48 dBµV/m
- At 30 MHz, I_{DM} = 28 dBµA, E_D = 0.3 µV/m = -10 dBµV/m

3. The maximum electric field produced by the common-mode current circulating along 2 wires is computed according to equation 4-25 :

$$\left|E_C\right|_{\max} = 1.257.10^{-6} \frac{L.f}{r} I_{CM}$$

Here, we suppose that the power supply cable is electrically short and we neglect the influence of the ground plane. Common-mode radiated emission at 3 meters:

- At 180 kHz, I_{DM} = 5 dBµA, E_D = 0.2 µV/m = -14 dBµV/m
- At 8 MHz, I_{DM} = 0 dBµA, E_D = 5 µV/m = 14 dBµV/m
- At 30 MHz, I_{DM} = 22 dBµA, E_D = 237 µV/m = 48 dBµV/m

4. Clearly, although the common-mode current is smaller than differential-mode current, the common-mode radiation is far larger than the differential-mode radiation. The following table compares the DM on CM current ratio and the DM on CM radiation ratio. This result proves that the common-mode current has a huge influence on radiated emission, and the circulation of a very small common-mode current cannot be neglected. It is not a surprise if common-mode current is the main root-cause of radiated emission problems. Common-mode conducted emission along long interconnects has to filtered strictly to prevent from unwanted radiated emission.

Frequency	DM on CM current ratio	DM on CM radiation ratio
180 kHz	40 dB	-68 dB
8 MHz	13 dB	-62 dB
30 MHz	6 dB	-58 dB

The limit EN55022 shown in Fig. 4-22 starts at 30 MHz, so the radiated emission below this frequency is not considered. At 30 MHz, the maximum electric field at 3 m is about 50 dBµV/m. The differential-mode radiated emission is far less than the limit and is not a concern for radiated emission compliance. In contrary, we evaluate that the common-mode radiated emission is only 2 dB below the limit and constitutes a serious issue for compliance to the radiated emission limit.

The measurement of common-mode current shown in Fig. 4-17 is a rapid and efficient method to detect likely radiated emission issue without performing a long and tedious radiated emission test. The conducted measurement shows a sharp resonance of the common-mode current about 30

MHz, which is associated to likely excessive radiated emission. This measurement also shows a similar resonance at 15 MHz.

V. EXERCISE NO 5 - Radiated susceptibility

A preliminary version of a multilayer PCB design is now ready and your next task is to identify likely EMC problems before the PCB fabrication. After a first review of the design, you pay attention to the two PCB traces which carry:

- a digital clock with the following characteristics: amplitude = 0-3.3 V, period = 40 ns, rise/fall time = 3 ns, the clock jitter should not exceed 1.5 ns
- an analog signal delivered to an 8-bit analog-to-digital converter, supplied under 3.3 V.

Both lines are routed on the top layer with microstrip configurations. They have exactly the same dimensions: the total length is 70 mm, the trace width is 0.25 mm, the height to reference plane is 0.38 mm. The traces are made of copper and designed on a FR4 board. The input and output impedances of circuits mounted at line terminals are unknown. They are assumed to be constant and equal to 150 Ω. The board has to undergo radiated susceptibility tests, where it will be illuminated by a harmonic plane wave whose maximum amplitude is 50 V/m, with frequency ranging from 80 MHz to 1 GHz.

1. Are the PCB traces electrically short?

2. Compute the worst-case amplitude of the voltage that will be induced on line terminals during the susceptibility test. Write out the assumption used for this evaluation.

3. Considering the circuits which are connected to PCB trace terminals, do you think that radiated disturbances may induce failures?

4. Which modifications of the PCB design could you suggest to mitigate radiated susceptibility problems?

Corrections:

1. A line is considered electrically short if its length is negligible compared to the wavelength. In practice, this assumption is assumed valid if the length L is less than a tenth of the wavelength. The electrically short condition is verified up to the following frequency:

$$F_{\max} = \frac{c}{10L\sqrt{\varepsilon_r}} = \frac{3.10^8}{10\times 0.07\sqrt{4.5}} = 200MHz$$

2. If the PCB traces are supposed electrically short and if the incoming wave is a plane wave, the voltages induced on line terminals can be evaluated according to equations 4-36 and 37. The field to line coupling depends on the incoming field orientation and polarization. As we consider a worst-case scenario, the field orientation shown in Fig. 4-30 is considered. The coupled voltages on each

terminal are not identical, so we will consider the terminal where the induced voltage is maximum. According to the previous assumptions, the worst-case coupled voltage amplitude varies linearly between 5 and 60 mV on the range 80 - 1000 MHz.

3. The first line is terminated by a digital clock input. A failure may occur if one of the two following conditions are verified:

- the amplitude of the induced voltage is large enough to change the logical state of the clock (bit flip)
- the induced voltage is translated into an excessive jitter and may lead to a timing error

As the voltage induced by the radiated disturbance has a negligible amplitude (80 mV) compared to the clock amplitude (3.3 V), the bit flip scenario is unlikely. The amount of induced jitter can be estimated according to equation 4-33. At 1 GHz, a sinusoidal voltage of 80 mV may create a jitter with an amplitude of 145 ps, which is ten times less than the maximum jitter requirement. We can conclude that the radiated disturbances do not degrade the clock signal enough to induce failure.

The second line is terminated by an analog-to-digital (ADC) input, whose resolution $\Delta = 3.3/2^8 = 13$ mV. At 1 GHz, if we neglect the likely filtering effect of the ADC input, the induced voltage is able to corrupt the third least-significant bits (LSB) of the converted word. The first LSB is completely corrupted above 200 MHz. A corruption of the conversion operation due to the coupling of the radiated disturbance on the PCB trace is a possible scenario.

4. The clock trace does not require any redesign from radiated susceptibility point of view. As an high speed signal is carried by this trace, radiation emission from this trace should be evaluated to decide if redesign should be done.

The risk of ADC disturbance is not negligible and a change of placement and routing is an efficient method to mitigate the radiated susceptibility issue. If possible, the line should be shortened as much as possible to reduce the coupled voltage. Another solution consists in shielding this sensitive trace: it consists burying the trace between two reference planes (power or ground).

VI. EXERCISE NO 6 - Identification of EMC problems

For the following integrated circuits, discuss the likely EMC related issues:

- Driver chip for a TFT LCD monitor
- Low-drop out linear voltage regulator
- Boost converter
- IEEE 802.15.4 Zigbee transceiver chip
- FPGA supporting numerous high speed interfaces
- LIN bus driver for automotive application

Corrections:

- Driver chip for a TFT LCD monitor: SI since it delivers high-speed signals. It is also a source of CE and RE since high-speed signals are carried to the screen through long interconnects.

- Low-drop out linear voltage regulator: immunity is a serious concern for this class of circui. In case of coupling of EM disturbance, rectification and DC offset generation can be induced,

that change the bias voltage of all the application. No emission problem since the regulation is not based on switched mode (linear regulation).

- Boost converter: it is a switched-mode power supply, so a large amount of transient current is generated and circulate along power supply cable harness i.e. CE. Interconnects acts as parasitic antenna so the boost converter is a potential source of RE. Due to the large amplitude command signals, SMPS are usually not susceptible devices.

- IEEE 802.15.4 Zigbee transceiver chip: as it is a RF receiver, it is sensitive to in-band interferences, so CI and RI are major issues for this class of circuit. Emission can be produced by RF transceiver and digital processing part, so CE and RE must also be addressed. SI is not an issue since low data rate is transmitted between Zigbee transceiver and baseband chip.

- FPGA supporting numerous high speed interfaces: FPGA is a large digital circuit with a large number of I/O buffers, so PI, CE and RE have to be addressed. Since this FPGA supports high-speed interface, SI must also be considered. Integrated circuits are immune to electromagnetic disturbance up to a certain level, so it is always possible to alter the operation of FPGA. As it is a digital IC, it remains less sensitive than RF or analog circuits. Priority should be given to PI, SI and RE issues.

- LIN bus driver for automotive application: CE and RE as it is a bus driver (low side driver). CI and RI also since electromagnetic noise coupled on LIN bus may degrade LIN bus driver performances. SI is not a major issue for LIN bus since it is a low data rate bus (max. 20 kbits/s).